Characterization of C^2MOS Flip-Flop in Sub-threshold Region

Baile Chen, Keye Sun
ECE 4332 – Fall 2009
University of Virginia
bf4m@virginia.edu, ks2kz@virginia.edu

ABSTRACT

In this paper, a timing model of Flip-Flop operation at sub-threshold region is used to characterize the C^2MOS Flip-Flop. It has been shown that optimum-timing design should be replaced by reliability-driven design for sub-threshold Flip-Flops. Size has effect on failure probability due to process variation. Also, Size has minor effect on the performance while supply voltage has large effect on performance due to its exponential character in current equation.

1. INTRODUCTION

As the integration level of the circuits becomes higher and higher, the power of the circuits becomes a major problem for modern VLSI designers. According to Moore's Law, the chip will be as hot as the rocket nozzle for the next few generations. As a result, Low-power integrated circuits become a major research topic in VLSI design field. Various technologies aiming at reducing the power of the circuits appear. Sub-threshold circuit is one of the attractive methods to reduce the circuit power in ultra-low power systems. As we know, the power of the digital gates is proportional to the square of the supply voltage. Thus reducing the supply voltage can result in a great reduction in power. So a large amount of research was focus on reducing the supplier voltage. When the supply voltage is reduced to sub-threshold region, MOSFETs come into cut off region. Then sub-threshold circuit concept comes onto the stage. The model for MOSFET in sub-threshold region is much different from the one in super-threshold region. The current is exponentially dependent on the gate-source and threshold voltage. So many modification and new design arise for the sub-threshold voltage circuits.

Timing is one of the most important issues in modern digital circuits. Flip-Flop is the most widely used timing blocks in digital circuits. Design of Flip-Flops is a important topic for circuit designer. When it comes into sub-threshold region, the design of Flip-Flops is more challenging due to large impact of process variation. The reliability problem is worsened dramatically when the supply voltage is reduced to sub-threshold region. A lot of work has been done on sub-threshold Flip-Flops. [1, 2, 3] Some timing models and characterization methods have been done to evaluate the performance of the sub-threshold Flip-Flops. [1] In this paper, we use the same characterization method to evaluate the C^2MOS Flip-Flop, which is one appropriate type of Flip-Flop operating in sub-threshold region.

2. C^2MOS FLIP-FLOP

The circuit schematic of C^2MOS FF is show in Fig.1. The C^2MOS FF is insensitive to clock overlaps due to the stacked PMOS and NMOS since the overlaps activate either the pull-up or the pull-down networks but never both of them simultaneously. The stacked PMOS and NMOS on the feedback loop cut off the ratio problem which should be

circumvented in sub-threshold circuits because process variation may result in wrong functionality. The stacked devices also reduce the off current I_{off} and increased the ration of on current to off current I_{on}/I_{off}. All these characteristics make C^2MOS FF suitable for sub-threshold application.

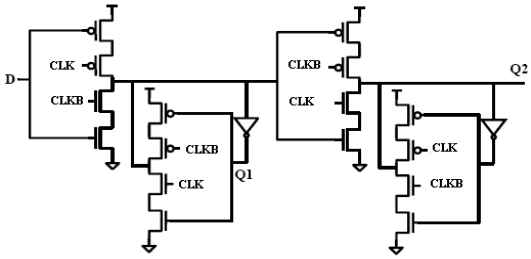
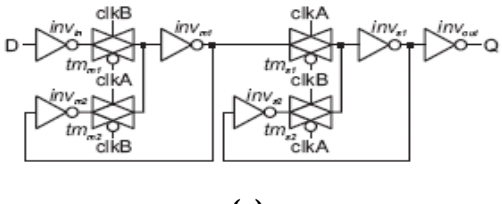


Fig 1. C2MOS FF circuit schematic

3. COMPARISON WITH DIFFERENT TYPES OF FLIP-FLOPS

To characterize the performance of C^2MOS FF, we compare the energy consumption and clk-to-Q delay of C^2MOS FF with other three types of conventional flip-flops. The three types of conventional flip-flip are transmission-gate flip-flop (TGFF), Semi-dynamic flip-flop (SDFF) and hybrid latch flip-flop (HLFF). The four flip-flop circuit schematics are shown in Fig.2.



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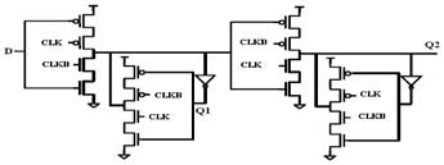

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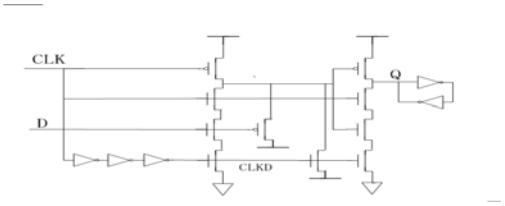

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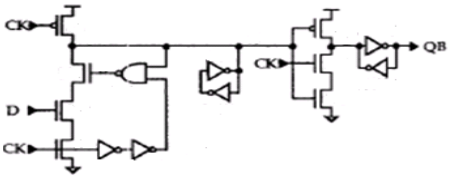
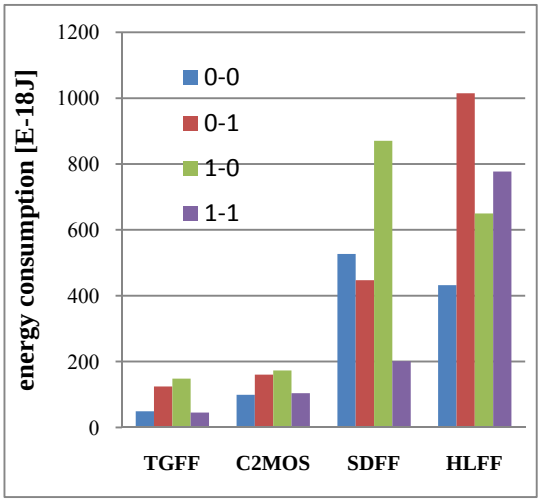
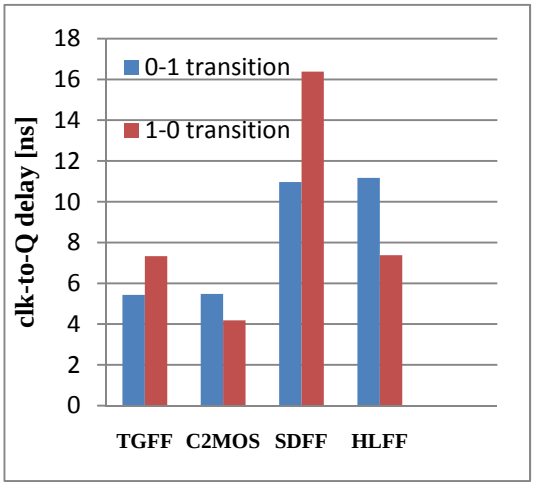


(d)

Fig.1. (a) TGFF (b) C^2MOS FF (c) SDFF (d) HLFF



(a)



(b)

Fig.3. (a) Energy consumption comparison of 4 types of FFs (b) clk-to-Q delay of comparison of 4 types of FFs

To compare the energy consumption, we get the values for all types of transitions (0-0, 0-1, 1-0, 1-1). [2] The results are show in Fig.3. We can see that the energy consumption of SDFF and HLFF are comparatively higher than TGFF and C^2MOS FF due to their glitching in pulse generation process. SDFF and HLFF sacrifice energy for performance. C^2MOS FF has a little higher energy consumption than TGFF. But C^2MOS FF has better performance than TGFF for its insensitivity to clock overlap. There is a good compromise between energy consumption and performance.

Fig.3 (b) shows the clk-to-Q delay of the four types of flip-flop. Both 0-1 and 1-0 transition are considered. We can see that the delay of SDFF and HLFF are higher than TGFF and C^2MOS. C^2MOS FF has a little lower clk-to-Q delay than TGFF. So C^2MOS FF is suitable for sub-threshold circuits which are slow.

3. TIMING AND ENERGY CHARACTERIZATION

Timing is a key point for correct functionality of flip-flops. So a good method for timing characterization is needed for flip-flop design. Various methods have been used in characterization of flip-flops. [1, 2, 3, 4] We use some of the method to characterize the C^2MOS FF operating in sub-threshold region.

3.1 SETUP TIME AND CLK-TO-Q DELAY

The model we used for sub-threshold region is shown in Fig.4. [1] The delay of the previous circuits, which is the input of flip-flop, has a lognormal probability distribution. [1] The lognormal distributed output of the combinational logic varies the setup time and hold time of the flip-flop, which is essential to the functionality. To determine how the setup time affects the operation, we have done several analysis on the effect of setup time on clk-to-Q delay and failure probability. The results are shown in Fig.5.

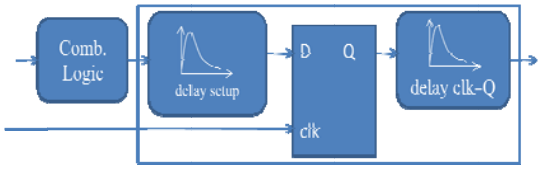


Fig.4. Timing model simplifying integration in environment

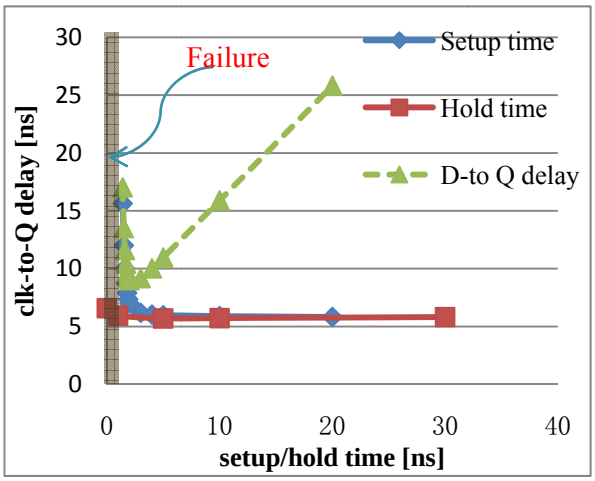


Fig.5. Dependence between setup/hold time and clk-to-Q delay

The clk-to-Q delay decreases with the increasing setup delay. Also, clk-to-Q delay decreases with increasing hold time. When setup time decreases to a certain value, the clk-to-Q delay increases drastically and becomes infinitely large. That corresponds to the failure of the flip-flop. But the failure situation doesn't appear for small hold time. This is not always the case. The same timing characterization has been done for TGFF and failure of operation occurs for small hold time. [1] D-to-Q delay has also been calculated as the addition of clk-to-Q delay and setup time. A minimum point can be seen on the curve, which is the optimum D-to-Q delay.

To see the process variation effect on the timing of the flip-flop, Monte-Carlo

simulation is used to see the relationship between setup time and clk-to-Q dealy. The result is shown on the Fig.6. The curve looks

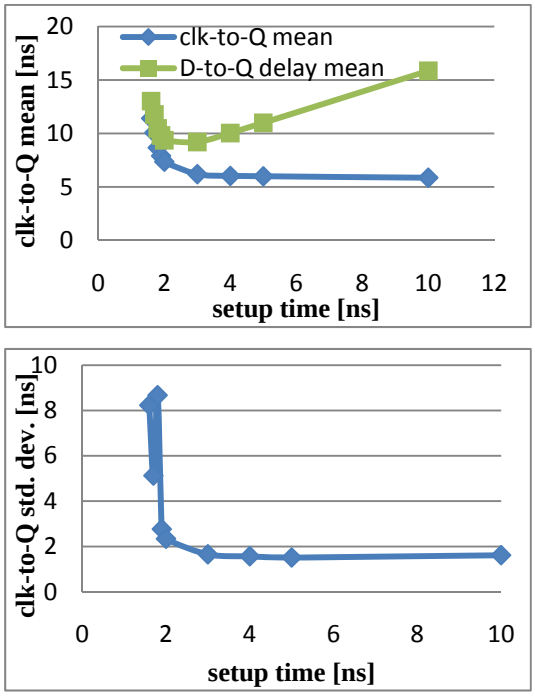


Fig.6. Dependence between clk-to-Q mean, standard deviation and setup time using Monte-Carlo method

the same as single simulation. The standard deviation decreases with increasing setup time. For smaller setup time, the standard deviation shows some random behavior due to failure of operation. The failure probability is also been calculated to show the relationship with setup time. The result is shown in Fig.7. We can see from the Fig.7 that for optimum D-to-Q delay, the failure probability is around 8%, which is too high for reliable operation. The 3σ corner, which defines the reliable region, set the setup time larger than about 4ns, which is larger than optimum D-to-Q delay point. So for a reliable design, 3σ corner should be chosen rather than optimum D-to-Q delay point. Thus a conclusion can be drawn that the sub-threshold flip-flop design becomes reliability-driven instead of optimum-timing driven.

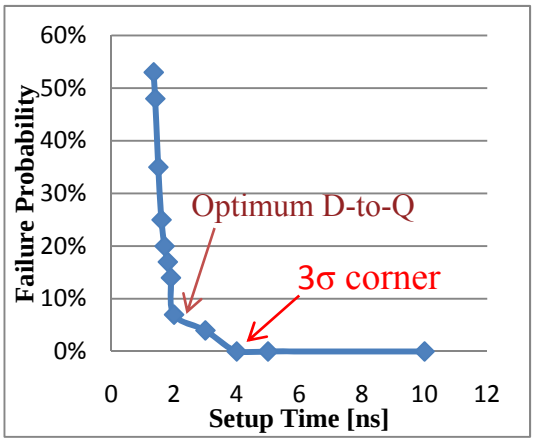


Fig.7. Dependence between failure probability and setup time

3.2 SUPPLY VOLTAGE AND SIZE EFFECT

Supply voltage and size are other two important knobs we can turn in circuit design. Dependence between energy consumption, delay and supply voltage has been calculated. The voltage effects on performance are shown in Fig.8. It can be seen that the energy per operation increased almost quadratically with increasing supply voltage for large supply voltage. That is predictable since the switching energy of digital circuits is quadratically dependent on the supply voltage and for large supply voltage the switch energy is the main source of power consumption. In theory, for very small supply voltage the energy consumption increases due to the exponentially increasing delay. [5] But the curve doesn't show that since the flip-flop fail to function correctly below about 0.18V. The dependence between clk-to-Q delay and supply voltage shows a decreasing delay with increasing supply voltage. This is also easily explained. Since the current charging or discharging the capacitances are exponentially dependent on the supply voltage while the voltage swing on the capacitances is only linearly dependent on supply voltage, according to equation (1), we can say that the delay decreases with increasing supply

voltage.

$$t_D = \frac{CV_{dd}}{I} \quad (1)$$

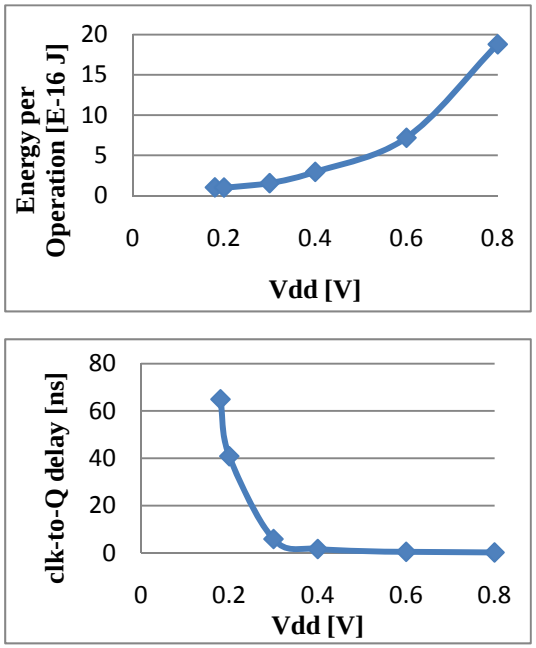
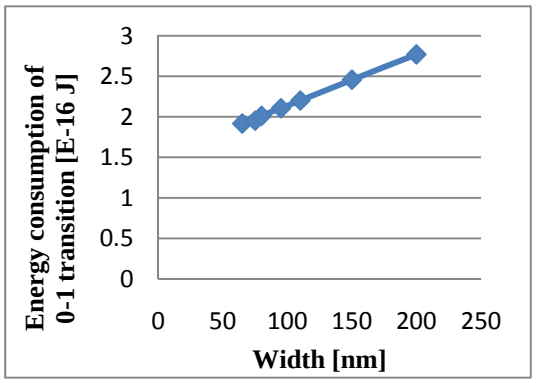


Fig.8. Dependence between energy, clk-to-Q delay and supply voltage

To determine the size effect on performance, we use the circuit shown in Fig.9. The width of PMOS is twice the width of NMOS. The results are shown on Fig.10. The energy consumption almost increases linearly with increasing sizes due to the increasing capacitances. The delay decreases with increasing sizes.



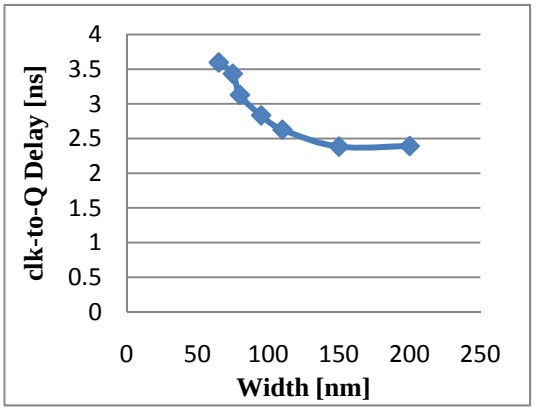


Fig.9. Dependence between energy consumption, clk-to-Q delay and device sizes

The relationship of failure probability and supply voltage for different sizes are shown on Fig.10. We test three circuits which have ratio of PMOS to NMOS 65nm:65nm, 130nm:65nm and 130nm:130nm. The failure probability are higher for 65:65 circuits than 130:130 circuits due to large process variation effect on small size devices. 130:65 circuits has the highest failure probability possibly because the process variation has unbalanced effects on strong and weak devices which makes the strong PMOS even stronger and weak NMOS even weaker. Also, we can see that supply voltage should be considered prior to sizes when designing flip-flop since it has large sensitivity on failure probability than sizes.

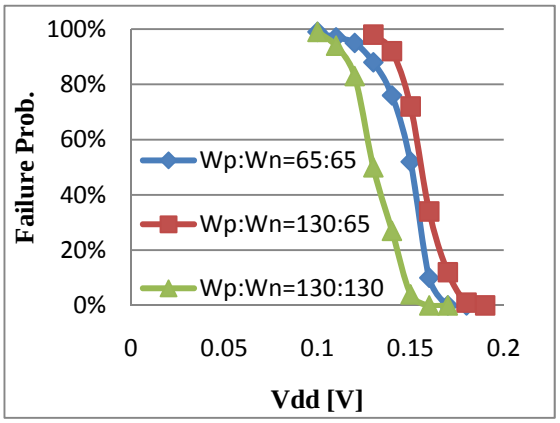


Fig.10. Dependence of failure probability and supply voltage for different sizes

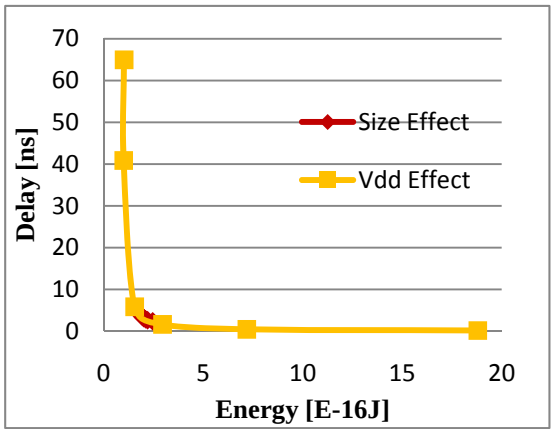


Fig.11. Dependence between delay and energy consumption of size effect and supply voltage effect

At last size effect and supply voltage effect on performance is compared. The results are shown on Fig.11. The curve for size effect only extends a small region compared to curve for supply voltage. So it can be said that size has smaller effect on the performance than the supply voltage. This is mainly because that size has only linear character in current equation while supply voltage has exponential one. This also confirms the conclusion we drawn before that supply voltage should be considered prior to size when designing sub-threshold flip-flop.

4. CONCLUSION

Timing and energy characterization has been done on performance of C^2MOS Flip-Flop operating in sub-threshold region. From the failure probability analysis, conclusion can be drawn that optimum-timing driven design, which is the conventional routine in super-threshold circuit design, should be replaced by reliability-driven design to ensure the correct functionality. Also, supply voltage has major effect on performance than size. When designing a sub-threshold circuits, supply voltage should be considered prior to size.

5. ACKNOWLEDGEMENT

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6. REFERENCES

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